Figure 6 shows the procedure of horizontal error correction in one sector.

Step (b-1): the same process as at step (a-1) in the prior art is performed except that not only the syndrome calculator 5 but also the error detector 7 are provided with instructions to transfer data.

Step (b-2): the DMA control unit 2 outputs the DMA request 13 to the bus control unit 3 so as to request the data transfer from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (b-3): the bus control unit 3 puts the data bus 11 in commission, and outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. The bus control unit 3 then outputs the syndrome data supply signal 15 and the error detector data supply signal 20 to the syndrome calculator 5 and the error detector 7, respectively, so as to supply the data read from the buffer memory 4 to the syndrome calculator 5 and to the error detector 7.

Step (b-4): the syndrome calculator 5 performs error-containing code detection for every transferred code word, and outputs the syndrome 16 to the error corrector 6. When an error-containing code word is detected, the syndrome calculator 5 outputs the error-containing code detection signal 22 to the error detector 7 and the system control unit 1, and also provides the system control unit 1 with the error-containing code word signal 23 indicating from which code word the error has been detected.

On the other hand, the error detector 7 also executes an error detecting process every code word. Only when the detection of an error-containing code is not informed by the error-containing code detection

signal 22, the error detector 7 stores the mid-term results of the error detection in every code word to the mid-term result register 8 whose response is quicker than memory. When the detection of the error-containing code has been informed, the error detector 7 does not perform error detection for the subsequent code words including the code word informed.

Step (b-5): the same process as at step (a-5) is performed.

Step (b-6): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read error-containing data therefrom. Then, the bus control unit 3 outputs the error corrector access signal 18 to the error corrector 6 to supply the data thereto.

Step (b-7): the same process as at step (a-7) is performed.

Step (b-8): after putting the data bus 11 in commission, the bus control unit 3 reads the error-corrected data from the error corrector 6 and overwrites the data in the buffer memory 4. When error correction for one sector is complete, the error corrector 6 transmits the correction completion signal 19 to the system control unit 1.

The above step (b-4) is executed in parallel with steps (b-5) through (b-8) like a pipeline.

Step (b-9): in order to check to see that the corrected data contain no more error, the system control unit 1 transmits the DMA command 12 to the DMA control unit 2 so as to provide instructions to transfer the data from the buffer memory 4 to the error detector 7. The system control unit 1 make the data transfer be started from the code word indicated by the

error-containing code word signal 23 outputted at the same time as the error-containing code detection signal 22 first outputted from the syndrome calculator 5 at step (b-4).

Step (b-10): the same process as at step (a-10) is performed.

Step (b-11): after putting the data bus 11 in commission, the bus control unit 3 outputs the buffer memory access signal 14 to the buffer memory 4 to read the data therefrom. Then, the bus control unit 3 outputs the error detector data supply signal 20 to the error detector 7 so as to supply the data read from the buffer memory 4.

Step (b-12): while using the mid-term results of error correction stored in the mid-term result register 8 as the initial value, the error detector 7 executes error detection for the transferred subsequent data, and informs the system control unit 1 of the presence or the absence of an error by transmitting the error detection signal 21.

When an error-containing code is not detected in the syndrome calculator 5 at step (b-4), the error correcting operations between steps (b-5) and (b-8) are performed in parallel with step (b-4) for code words in descending order of stream; however, error correction for the data on the buffer memory 4 is not performed because an error-containing code has not been detected. The error detecting process done by the error detector 7 is complete at step (b-4), and the error detection signal 21 is transmitted to the system control unit 1 so as to indicate whether an error has been detected or not. In this case, steps (b-9) through (b-12) are not executed.

Through these steps, the horizontal error correction for one sector is complete. In the same manner, horizontal error correction for the